



Doc No : - ASSC/110/5/2*

Issue 2 – June 2000

ENGINEERING BULLETIN ON THE OPERATION OF DEF STAN 00-18 (PART 2)/US MIL-STD-1553B DATA BUSES AT ENHANCED DATA RATES

SUMMARY

Future avionic systems update programmes will require data throughputs in excess of that provided by Def Stan 00-18 (Part 2)/US MIL-STD-1553B bus networks. However, upgrading to new bus systems that require the installation of new cable networks within the airframe would be extremely costly and time consuming, since de-skinning the airframe would often be required.

A more cost effective solution would be to operate existing installed electrical Def Stan 00-18 (Part 2)/US MIL-STD-1553B bus networks at greater signalling speeds than the currently specified 1 Mbit/s, so as to offer a greater throughput without the need to modify the networks themselves.

This engineering bulletin summarises the investigations carried out by ASSC and provides guidance on the issues involved in the operation of installed Def Stan 00-18 Part 2/US MIL-STD-1553B data bus networks at enhanced bit rates.

The text concentrates on achievement of modest improvements in bit rate (target 5Mbit/s) with minimal modifications to terminal hardware. A brief summary of work undertaken by SAE NG1553 (target 100Mbit/s), using more radical modifications to terminal hardware is given in Appendix A.

* This report is published by the Avionic Systems Standardisation Committee (ASSC) to advance the role of standardisation in avionics. The use of this is entirely voluntary, and its applicability and suitability for any particular use, including any patent infringement arising therefrom, is the sole responsibility of the user. Copies of this paper are obtainable from the ASSC Agency as an Avionic Systems Standardisation Committee publication. Copies of this paper are obtainable from the ASSC Agency as an Avionic Systems Standardisation Committee publication.

Appendix B provides example calculations on terminal timing parameters versus maximum bus length.

It is intended that this bulletin will be updated in due course to reflect future developments.

Table of contents	Page no.
SUMMARY	I
RELATED DOCUMENTS	V
GLOSSARY	VI
1 INTRODUCTION	1
2 BACKGROUND	1
2.1 The problem	1
2.2 Potential solutions	1
2.2.1 Enhanced bit rate Def Stan 00-18 Part 2/US MIL-STD-1553B based solutions	2
2.2.2 Non-Def Stan 00-18 Part 2/US MIL-STD-1553B based solutions	2
2.3 Combined high and standard bit rate solutions	2
3 SUMMARY OF ASSC DATA INTERFACES SUBCOMMITTEE INVESTIGATIONS	3
3.1 Phase 1	3
3.2 Phase 2	3
3.3 Phase 3	3
4 BUS HARDWARE ISSUES AFFECTING OPERATION AT ENHANCED BIT RATES	4
4.1 Couplers	4
4.2 Bus cable	5
4.3 Stubs	5
5 TERMINAL PERFORMANCE ISSUES AFFECTING OPERATION AT ENHANCED BIT RATES	7
5.1 Isolation Transformers	7
5.2 Transceivers	7
5.3 Protocol devices	8
5.3.1 Clock/bit rate	8
5.3.2 Terminal related timing issues	8
5.4 Sub-system interface	9
6 ENVIRONMENTAL ISSUES	10
6.1 EMC	10
6.2 Temperature	10

Table of contents (cont)	Page no.
7 DEVELOPMENT OF STRATEGIES FOR OPERATION OF DEF STAN 00-18 (PART 2)/US MIL-STD-1553B DATA BUSES AT ENHANCED BIT RATES	10
APPENDIX A – TERMINAL TIMING PARAMETERS VERSUS BUS LENGTH - EXAMPLE CALCULATIONS	12
APPENDIX B - ‘RADICAL’ APPROACHES	16
FIGURES	
Figure 1: Effects of Transceiver and Bus Propagation Delays	14
TABLES	
Table 1: Terminal timing parameters specified by Def Stan 00-18 Part 2/US MIL-STD-1553B	12
Table 2: Timing Parameter Values for Various Data Rates – Extreme Case	15
Table 3: : Timing Parameter Values for Various Data Rates – More Probable Case	15

RELATED DOCUMENTS

Def Stan 00-18 (Part 2)/Issue 2, Serial Time Division Command/Response Multiplex Data Bus Standard, September 1990.

MIL-STD-1553B with Notice 2, Digital Time Division Command/Response Multiplex Data Bus, 8 September 1986.

STANAG 3838 AVS Digital Command/Response Multiplex Data Bus

SAE AS15531 Digital Command/Response Multiplex Data Bus, November 1995

Study of Maximum Signalling Speed for Def Stan 00-18 (Part 2)/US MIL-STD-1553B Data Buses, ASSC/110/2/85, February 1997.

Further Study of Maximum Signalling Speed for Def Stan 00-18 (Part 2)/US MIL-STD-1553B Data Buses, ASSC/110/2/97, March 1998.

Continued Study of Maximum Signalling Speed for Def Stan 00-18 (Part 2)/US MIL-STD-1553B Data Buses, ASSC/110/2/111, February 1999.

BAe Military Aircraft – Some Def Stan 00-18 (Part 2) Data bus Configurations, ASSC/110/2/92, May 1997.

GLOSSARY

ASD	Avionic Systems Division (of SAE)
ASSC	Avionic Systems Standardisation Committee
BC	Bus Controller
CAP	Carrier Amplitude Phase (modulation)
DMT	Discrete Multi Tone (modulation)
DSL	Digital Subscriber Line
EMC	Electromagnetic Compatibility
MACAIR	Standard issued by the McDonnell Douglas aircraft company
Mbit/s	Mega bits per second
NG1553	Next Generation 1553 Task Group (of SAE ASD)
PC	Personal Computer
QAM	Quadrature Amplitude Modulation
RT	Remote Terminal
SAE	Society of Automotive Engineers
SDMT	Synchronous Discrete Multi Tone (modulation)
UK	United Kingdom
VME	Versa Module Europa - a backplane interconnection bus system standardised as IEEE 1014-1987.

1 INTRODUCTION

This engineering bulletin is intended to provide guidance on the operation of Def Stan 00-18 Part 2/US MIL-STD-1553B data bus network hardware at bit rates in excess of the 1 Mbit/s defined in the standard.

This guidance is based on:

- * investigations carried out by the Data Interfaces Subcommittee of ASSC
- * feedback received from SAE ASD AS-1 NG1553 Task Group
- * information received from various other industry sources.

2 BACKGROUND

2.1 The problem

Over the last two decades Def Stan 00-18 Part 2/US MIL-STD-1553B has become by far the most widely used standard in the world for military avionic data bus systems. However, modern avionic systems are subject to ever-increasing demands for rapidly moving large volumes of data, and thus require bandwidths in excess of the 1 Mbit/s defined in the standard. These demands exist in both new aircraft and in update programmes, and it is the latter that are the main subject of this bulletin.

The obvious solution is to install new data bus systems specified to provide higher bandwidth, and work is in progress (outside the scope of this bulletin) to identify and implement appropriate standards. Such standards invariably define different media hardware to that defined by Def Stan 00-18 Part 2/US MIL-STD-1553B.

In the case of updates to the avionic systems in existing aircraft the replacement of the installed Def Stan 00-18 Part 2/US MIL-STD-1553B bus hardware would almost always require de-skinning of the aircraft and would therefore be extremely costly. A preferable solution would be to utilise existing installed bus hardware for transmission of data at higher bit rates. Surveys have shown that, in most cases, the inaccessibility of bus hardware (most specifically couplers), makes it essential that the installed bus hardware be utilised with no modification whatsoever.

This engineering bulletin summarises the issues involved in operating standard Def Stan 00-18 Part 2/US MIL-STD-1553B bus hardware at enhanced bit rates and reviews some of the work that has been carried out as of January 2000.

2.2 Potential solutions

Simplistically there are two fundamentally different approaches to the operation of Def Stan 00-18 Part 2/US MIL-STD-1553B bus networks at enhanced bit rates, as follows.

2.2.1 Enhanced bit rate Def Stan 00-18 Part 2/US MIL-STD-1553B based solutions

The first approach is to retain the signalling method (Manchester bi-phase encoding), word formats, message formats and protocols defined in the standard and simply operate at higher bit rates. The investigations undertaken by ASSC Data Interfaces Subcommittee have concentrated mostly on this 'conservative' approach. The objective has been to achieve modest bit rate enhancements (target 5Mbit/s) with minor modifications to terminal hardware.

2.2.2 Non-Def Stan 00-18 Part 2/US MIL-STD-1553B based solutions

The second, more radical approach, is to investigate the potential of completely different techniques, for example those used in the telecommunications industry for transmission of data over relatively poor quality telephone lines. This approach is likely to require radical redesign of terminal hardware, but may offer the prospect of considerably greater bit rate enhancement. The work carried out by the SAE ASD AS1-A NG1553 Task Group has concentrated mostly on such 'radical' potential solutions.

A brief summary of the work undertaken by NG1553 is given in an appendix to this bulletin.

2.3 **Combined high and standard bit rate solutions**

It is envisaged that future systems may include terminals operating at both the current standard 1 Mbit/s and at higher bit rates, the higher bandwidth being achieved by either 'conservative' or 'radical' approaches. The benefits arising from such an arrangement include the ability to retain terminal equipment designed to meet the current 1 Mbit/s standard and, in cases where the existing network is to be extended, the ability to implement a greater number of Remote Terminal addresses. The actual number of extra RT addresses would depend on the technique adopted. In the case of the 'conservative' approach it might be possible to double the number of RTs to 62. However, it is possible that electrical loading imposed on the bus by additional stubs would limit the number to less than this.

3 SUMMARY OF ASSC DATA INTERFACES SUBCOMMITTEE INVESTIGATIONS

The objective of the work undertaken by ASSC Data Interfaces Subcommittee has been to achieve modest bit rate enhancement (target 5 Mbit/s) with minor modifications to terminal hardware.

The investigations were performed in three phases as follows.

3.1 Phase 1

The first phase consisted of relatively simple tests using function generators to try and determine the probable behaviour of bus networks at high bit rates.

Hardware from one supplier was used to implement a 9.8m long bus with 8 transformer coupled stubs each 2m long. The signals observed suggested that the bus might be expected to function at frequencies (and hence bit rates) up to between 8 and 10 MHz.

A second bus was implemented using hardware from a second supplier with a bus length of 36m and 9 stubs, with various lengths from 1.3m to 4m. Tests indicated that this bus might be expected to function at frequencies up to 6 MHz.

3.2 Phase 2

In the second phase a test system was implemented with a bus controller (BC), remote terminal (RT) and a VME card PC computer to control and monitor the functioning of the BC and RT. Provision was made to vary the clocking frequency of the terminal protocol devices, and hence the bit rate. The terminal transceivers were modified by removal of the receiver input filter capacitors to ensure functionality at higher bit rates than 1Mbit/s. The transceiver transmitters were unmodified.

Tests were performed on the 9.8m long 8 stub bus described in 3.1 above, and showed that the terminals were able to communicate between the stubs furthest apart (9.8m) at bit rates of up to 2.8Mbit/s, albeit with significant distortion of the received waveform. This distortion is believed to be due to the combined effects of limits on transceiver output slew rate and bus hardware filtering effects. In fact the maximum bit rate was constrained by limitations in the clocking arrangements for the protocol devices, rather than by the bus hardware.

3.3 Phase 3

In the third phase the terminal protocol device clocking arrangements were improved and it became possible, by selection, to achieve bit rates in excess of 5Mbit/s. However at 5 Mbit/s the terminal output waveform was subject to significant distortion due to transmitter output slew rate constraints.

Additional software was produced to provide monitoring and display of error rates.

Tests were performed using bus hardware from two suppliers in the following three configurations (six buses total):

- * short (1.2m) bus with eight long (6.1m) stubs
- * average (9.7m) bus with eight average (3m) stubs
- * long (30m) bus with eight short (0.6m) stubs.

These bus arrangements were selected to cover the range defined in ASSC/110/2/92, a paper on bus configurations in use in UK aircraft.

Tests were performed to determine the bit rate at which errors started to occur. This ranged from 2.5 Mbit/s for one of the long bus implementations to 4 Mbit/s for one of the medium buses and one of long buses.

Tests were also performed to try and determine the constraints imposed by various bus hardware elements. Signals were injected into various bus hardware parts using the Bus Controller (with MIL-STD-1553B transceivers modified as described in 3.2 above), RS422 line drivers and function generators. The effects on signal waveform were observed and recorded.

4 BUS HARDWARE ISSUES AFFECTING OPERATION AT ENHANCED BIT RATES

This section summarises the findings of the investigations carried out by ASSC Data Interfaces Subcommittee, together with information from other sources, regarding the issues that need to be addressed when considering the utilisation of Def Stan 00-18 Part 2/US MIL-STD-1553B bus hardware at data rates in excess of the standard 1 Mbit/s using the 'conservative' approach.

It is impossible to make definitive general statements about the performance of bus hardware at bit rates above 1 Mbit/s since there are many, suppliers each with a variety of products. These products were designed to meet the requirements of the standard at 1 Mbit/s with no regard for performance at higher bit rates, and hence products from different suppliers, or different products from the same supplier, may exhibit different behaviour at high bit rates.

4.1 Couplers

Transformer couplers may be the most important element in the bus network in terms of their effect on signal waveform.

Tests performed by ASSC Data Interfaces Subcommittee (and by various coupler suppliers) indicate that most couplers exhibit only a small increase in insertion loss up to about 2 MHz with varying rates of increase with frequency thereafter. Some coupler types have frequency responses that fall off by about 2.5dB between 1 MHz and 5 MHz, while others have flat responses up to much higher frequencies.

The fact that the insertion loss of a coupler increases with frequency does not necessarily render its use at higher bit rates unfeasible. Tests suggest that, depending on the bus configuration (e.g. bus length, number and lengths of stubs etc.), it may be possible to operate some bus networks at bit rates of up to 5 Mbit/s even if coupler response has started to fall off. In practice the biggest problem is likely to be due not to reduced amplitude, but to distortion introduced during transitions from low frequency parts of the waveform (e.g. sync pattern) to high frequency parts (e.g. data bits). However, it is worth noting that some other investigators have declared that a simple 'faster 1553' approach will not work satisfactorily above 2 Mbit/s.

There have been suggestions that couplers should be modified for operation at higher bit rates. However, the inaccessibility of couplers installed in aircraft makes this approach unacceptable in most cases.

4.2 Bus cable

The obvious problem with bus (and stub) cable is that attenuation generally increases with frequency, since the cable acts as a low pass filter. Tests performed by ASSC Data Interfaces Subcommittee on a limited sample of cable indicate a roughly linear increase in attenuation (in dB) relative to frequency from 1 MHz to about 50 MHz. It is understood from other sources that in some cases the characteristics (e.g. characteristic impedance, surface transfer impedance etc.) of cables designed for 1 MHz operation are unpredictable and subject to significant variations at higher frequencies.

Reports have been received of problems with Voltage Standing Waves causing amplitude variations on long buses at high bit rates. It is reported that the problems occur with bit rates above about 4 Mbit/s and bus lengths of 60m or more. While such bus lengths might be thought to apply to only a few very large aircraft types ¹, it should be noted that buses may be twice as long as the aircraft. Hence it is important to recognise this and other potential problems related to long buses.

Other issues that may be relevant in the case of long buses are those of propagation delay compared with minimum no-response time out, response time and intermessage gap time. This is discussed in 5.3.2 and in Appendix A.

4.3 Stubs

To characterise the performance at high bit rates of stubs connected to the transmitting terminal, tests were performed on a 6.1m stub terminated in a coupler connected to a dummy bus consisting of 2 bus terminating resistors. For most types of coupler the

¹ Lockheed C-130 Hercules: length 29.6m, wingspan 40.2m
 Boeing C-17 Globemaster III: length 53m, wingspan 51.8m
 Boeing 747-400: length 70.7m, wingspan 64.4m
 Antonov An-225: length 84m, wingspan 88.4m (world's largest aircraft)

variation with frequency in amplitude received at the stub side of the coupler was relatively flat up to 5 MHz, but with significant peaking thereafter.

Stubs impose impedance on the bus that reduces as stub length increases. It has been shown that at 1 MHz a 6.1m long² transformer coupled stub imposes an impedance of less than 600 Ω on the bus, thus if a number of such stubs are attached to a bus significant loading and impedance mismatch is created. Furthermore, stub cables exhibit largely capacitive impedance and hence they will have even lower impedance at higher frequencies/bit rates.

² The maximum length limit recommended by Def Stan 00-18 Part 2/US MIL-STD-1553B.

5 TERMINAL PERFORMANCE ISSUES AFFECTING OPERATION AT ENHANCED BIT RATES

This section reviews the findings of the investigations carried out by ASSC Data Interfaces Subcommittee, and the issues that need to be addressed when considering the utilisation of Def Stan 00-18 Part 2/US MIL-STD-1553B terminal hardware at data rates in excess of the standard 1Mbit/s using the 'conservative' approach.

5.1 Isolation Transformers

The isolation transformers mounted within terminals between transceivers and stub are often of similar design to coupling transformers, and therefore liable to suffer the same problems when used at high bit rates. However, the designer is able to replace the isolation transformers, an option that is generally not available in the case of coupling transformers.

5.2 Transceivers

Predictably, ASSC's investigations have shown that transceivers designed for 1Mbit/s operation are unlikely to perform satisfactorily at higher bit rates.

Both receivers and transmitters need to be modified to handle the higher frequencies associated with higher bit rates.

So far (June 2000) tests have only been performed by ASSC Data Interfaces Subcommittee with transceivers having modified receiver input filters, modification consisted of simply removing the filter capacitors.

The waveform rise and fall times of typical transmitters designed for 1Mbit/s operation are such that at bit rates above about 2Mbit/s the edges merge, and the transmitted amplitude is reduced. Clearly, faster slew rate is most desirable in order to achieve acceptable operation. The optimum rise and fall times are debatable, and will be a compromise between the need to avoid signal attenuation and the need to minimise electromagnetic emissions due to fast transients. It is probable that slew rates that ensure that the waveform produced from a series of '1s' or '0s' approximates to a sine wave would be appropriate. Indeed there may be a case for aiming for a sinusoidal output as used in various 1553 like MACAIR standards. A sinusoidal waveform should result in minimised electromagnetic emissions and waveform distortion. It is often observed, on standard 1Mbit/s bus networks, that waveforms received at terminals do in any case approximate to a sine wave after traversing the bus network.

ASSC's investigations have been hampered by lack of transceivers with fast slewing transmitter outputs. As of June 2000 tests with transceivers modified as discussed above are still under consideration.

Transceivers impose further important constraints on operation at enhanced bit rates, due to the propagation delays in both transmitters and receivers. For transceivers designed for use at 1Mbit/s, this is typically of the order of 750ns total for transmitter and receiver combined. Receivers with input filters modified for use at higher bit rates may exhibit reduced propagation delay, but no data on this is currently (June 2000) available.

Section 5.3.2.1 below discusses the implications of transceiver propagation delay for terminal operation.

5.3 Protocol devices

5.3.1 Clock/bit rate

It appears likely that in most cases the protocol elements of terminals intended for operation at modestly enhanced bit rates could be implemented using existing devices simply by increasing the device clock rate. ASSC's investigations showed that selected protocol and encoder/decoder devices from one supplier could be made to function at bit rates of 5Mbit/s by increasing the frequency of the clock signal from 16MHz to 80MHz. Some devices use lower clock frequencies (e.g. 6 or 10MHz) and this may make enhanced bit rates easier to achieve.

The device type tested by ASSC was of a mature design and it is considered possible that newer devices with smaller feature sizes might function at still higher clock frequencies, and hence bit rates. However, no other devices have yet been evaluated.

5.3.2 Terminal related timing issues

5.3.2.1 Response Time, Minimum No-response Timeout and Inter-message Gap Time

In most designs the values of the above parameters measured at the protocol device are inversely proportional to device clock frequency. So that, for example, a remote terminal protocol device with a response time of 10us at 1Mbit/s would have a response time of 5us at 2Mbit/s. Clearly the terminal designer should confirm the proportionality of these timing parameters with respect to clock and bit rate.

However, the values of the above parameters measured at the terminal to stub connection are influenced by the fixed (not proportional to clock rate) transceiver propagation delay discussed in 5.2 above. Hence the Response Time of a complete remote terminal is equal to that of the protocol device plus the propagation delay of its transceiver (both receiver and transmitter). The Minimum No-response Timeout of a complete bus controller is equal to that of the protocol device minus the propagation delay of its transceiver.

Consideration must also be given to the time taken for signals to propagate along the bus between terminals compared with these timing parameters. The time available for the round trip propagation is equal to the difference between Minimum No-response Timeout of the bus controller and the Response Time of the remote terminal, while the

propagation time is dependent upon the bus length and the velocity of propagation in the bus cable.

Appendix A provides detailed examples of some relevant timing calculations to demonstrate the above problem.

These issues relate equally to BC to RT and RT to BC message formats. Furthermore, since the RT to RT validation requirement in Notice 2 to US MIL-STD-1553B implies the same Minimum No-response Timeout³ as for BC to RT message format, the same arguments apply to RT to RT transfers.

A possible solution to these problems would be to modify the protocol device design so that the relevant timing parameters are not simply reduced from the standard 1Mbit/s values in proportion to the bit rate, but are given values that ease the constraints discussed above.

5.3.2.2 Terminal fail safe

Def Stan 00-18 Part 2/US MIL-STD-1553B requires that terminals shall implement a terminal fail-safe timeout to preclude signal transmission in excess of 800us (at 1Mbit/s). Clearly this needs to be taken into account when operating at enhanced bit rates.

It is understood that some terminal devices are designed such that the fail-safe timeout is inversely proportional to clock/bit rate. Others have hardware that prohibits transmission of more than 33 words. In both these cases the fail-safe timeout may be expected to provide appropriately timed protection at higher bit rates.

However, some terminal designs rely on a monostable circuit to provide the fail-safe timeout. In this case the monostable timing components would have to be changed to provide an appropriate fail-safe timeout at enhanced clock/bit rates.

5.4 **Sub-system interface**

Operation of terminals at enhanced bit rates only makes sense if it is possible to transfer data between terminals and their subsystems fast enough to prevent the subsystem interface becoming a 'bottle neck'.

The devices used in the tests performed for ASSC Data Interfaces Subcommittee are capable of operating either by accumulating incoming data words in registers ready for transfer to the subsystem after message validation; or by transferring each word to the subsystem in turn as it is received. Converse arrangements are available for data to be transmitted.

³ If measured between the last zero crossing in transmit command word and the sync zero crossing in the status word from the transmitting RT.

Since it is most desirable that terminals should be capable of receiving successive messages separated only by brief inter-message gaps, the latter of the above two approaches would seem most appropriate for achieving rapid transfer of data across the subsystem interface. However, a greater degree of terminal - subsystem hardware integration would be required.

6 ENVIRONMENTAL ISSUES

6.1 EMC

The acid test, which all candidate solutions have to pass, is EMC.

Clearly changes in bit rate, signal levels, encoding/modulation techniques or transmitted frequency spectrum are likely to effect the electromagnetic characteristics of bus systems, both in terms of emissions and susceptibility.

Depending on the techniques adopted cables may be required to convey signals at frequencies well above those they were designed for, with a consequent risk of excessive emissions.

Furthermore, lower signal levels, waveform distortion and complex modulation techniques may lead to reduced tolerance to interference. i.e. poorer susceptibility than the standard systems.

6.2 Temperature

There is a risk that either bus or terminal hardware might exhibit changes in behaviour with temperature that would impair system performance at enhanced bit rates. This is particularly the case when components or devices are used outside their original design envelope.

7 DEVELOPMENT OF STRATEGIES FOR OPERATION OF DEF STAN 00-18 (PART 2)/US MIL-STD-1553B DATA BUSES AT ENHANCED BIT RATES

Clearly the first stage in development of any data transmission system should be a rigorous requirements capture. This should start at a high level defining requirements including data volumes, latency and determinism and lead eventually to a gross data rate requirement.

A fundamental problem in using existing bus networks at high bit rates is that the bus hardware is being used in ways it was never designed for. Hence a vital part of any programme to implement enhanced data rate communication is to define the characteristics of the installed bus network in relation to the characteristics of the signals that it is proposed should be transmitted. This should include investigating the effects of any variations in the build standard (e.g. use of different materials and components in

different batches and production runs). The effects of temperature on bus hardware should also be addressed, this may require thermal testing on sample parts.

The above comments apply equally to terminal hardware. Before committing to the use of protocol devices at bit rates above their original design speed a rigorous programme of testing should be undertaken to verify the probable reliability and yield. This should also include thermal testing, since it is likely that the ability of devices to operate at enhanced bit rates will be temperature dependent.

Other tasks should include:

- Evaluating and comparing the performance of different potential solutions against the requirement and against the installed network characteristics, this may include modelling of candidate solutions.
- Consideration of terminal timing issues with regard to long buses.
- Functional prototype evaluation and testing (including error rates).
- EMC testing.

APPENDIX A – TERMINAL TIMING PARAMETERS VERSUS BUS LENGTH - EXAMPLE CALCULATIONS

This appendix illustrates the effects of reducing terminal protocol device Response Time, Minimum No-response Timeout and Inter-message Gap Time from the standard 1Mbps values in proportion to the bit rate, together with the effects of the fixed (not variable with clock frequency) delays due to transceivers and bus propagation.

Def Stan 00-18 Part 2/US MIL-STD-1553B specifies (for 1Mbit/s operation) the minimum and maximum values of the above parameters as shown in Table 1.

Parameter	Minimum (us)	Maximum (us)
RT Response Time	4	12
BC No-response Timeout	14	not specified
BC Inter-message Gap Time	4	not specified

Table 1: Terminal timing parameters specified by Def Stan 00-18 Part 2/US MIL-STD-1553B

Note that:

- RT Response Time is measured at the RT's connection to its stub and is the time between the zero crossing of the command word parity bit and the zero crossing at the centre of the status word sync pattern.
-
- BC No-response Timeout is measured at the BC's connection to its stub and is the time between the zero crossing of the command word parity bit and the zero crossing at the centre of the expected status word sync pattern.
-
- BC Inter-message Gap Time is measured at the BC's connection to its stub and is the time between the zero crossing of the command word parity bit and the zero crossing at the centre of next command word sync pattern.
-

Inter-message Gap Time is usually controllable via the BC subsystem interface and is therefore unlikely to be a problem. Hence this discussion concentrates on Response Time and No-response Timeout and the relationship between them.

When measured at their respective protocol devices the above parameters will in most designs be inversely proportional to device clock frequency. However, when measured at the terminals' inputs/outputs they will be modified by the fixed delays in the terminal transceivers. These effects are illustrated in Figure 1, for simplicity a mode command without data word message format is shown. It can be seen that the RT Response Time is increased by the transceiver delay and the BC No-response Timeout is reduced by the transceiver delay, compared with the values at the protocol devices.

The time available for bus propagation is equal to the difference between Minimum No-response Timeout (at BC input/output) and Response Time (at RT input/output). Comparing Maximum Response Time with Minimum No-response Timeout in Table 1, it can be seen that (at 1Mbit/s) the minimum time available for round trip propagation between terminals is 2us. The propagation velocity of signals along the bus depends on the physical characteristics (principally characteristic impedance and capacitance per unit length) of the bus cable. This is generally in the order of 2×10^8 m/s, constraining the bus length to about 200m for 2us propagation time.

If Response Time etc. at the protocol device are proportional to clock rate, then as bit clock/bit rate is increased both the absolute values of No-response Timeout and Response Time, and the margin between them decrease. However, the value of Response Time and No-response Timeout at the terminal input/output are modified by the fixed transceiver delays. Table 2 and Table 3 show some illustrative numbers.

Table 2 represents the extreme (and unlikely) case where the RT protocol device has been designed such that at 1Mbit/s the terminal just achieves the maximum allowed Response Time of 12us (measured at its input/output), and the BC imposes the minimum permissible No-response Timeout of 14us (measured at its input/output). A transceiver delay of 0.75uS has been assumed for both the RT and BC. The final column shows the maximum bus length for each bit rate, assuming a commonly used yardstick for propagation time per unit length of 5.28ns/m (1.6ns/ft). It can be seen that the effect of the transceiver delay is such that at about 2.5Mbits/s the Response Time of the RT exceeds the No-response Timeout of the BC. This implies that in such a situation a Bus Controller could register a no-response even if the Remote Terminal had transmitted a status word. Furthermore, since the standard does not define the timing of a Bus Controller's subsequent transmissions following a no-response it is possible that the Bus Controller could transmit another command word while the status word is propagating along the bus.

The above discussion assumes the worst case combination of longest permissible Response Time and minimum No-response Timeout. However, experience suggests that many terminals are designed with a Response Time of around 10us, rather than the 12us maximum permitted. Terminals may also be designed to provide No-response Timeouts longer than the 14us minimum. This means that in practice the timing and bus length constraints may be less onerous than those discussed above.

Table 3 represents a more likely case where the RT has been designed such that at 1Mbit/s it achieves a Response Time of 10us (measured at its input/output) and the BC imposes a No-response Timeout of 16us (measured at its input/output). Again a transceiver delay of 0.75uS has been assumed for both the RT and BC. It can be seen that in this case the effect of the transceiver delay is such that a bit rate up to 5Mbits/s can be achieved before the Response Time of the RT equals the No-response Timeout of the BC.

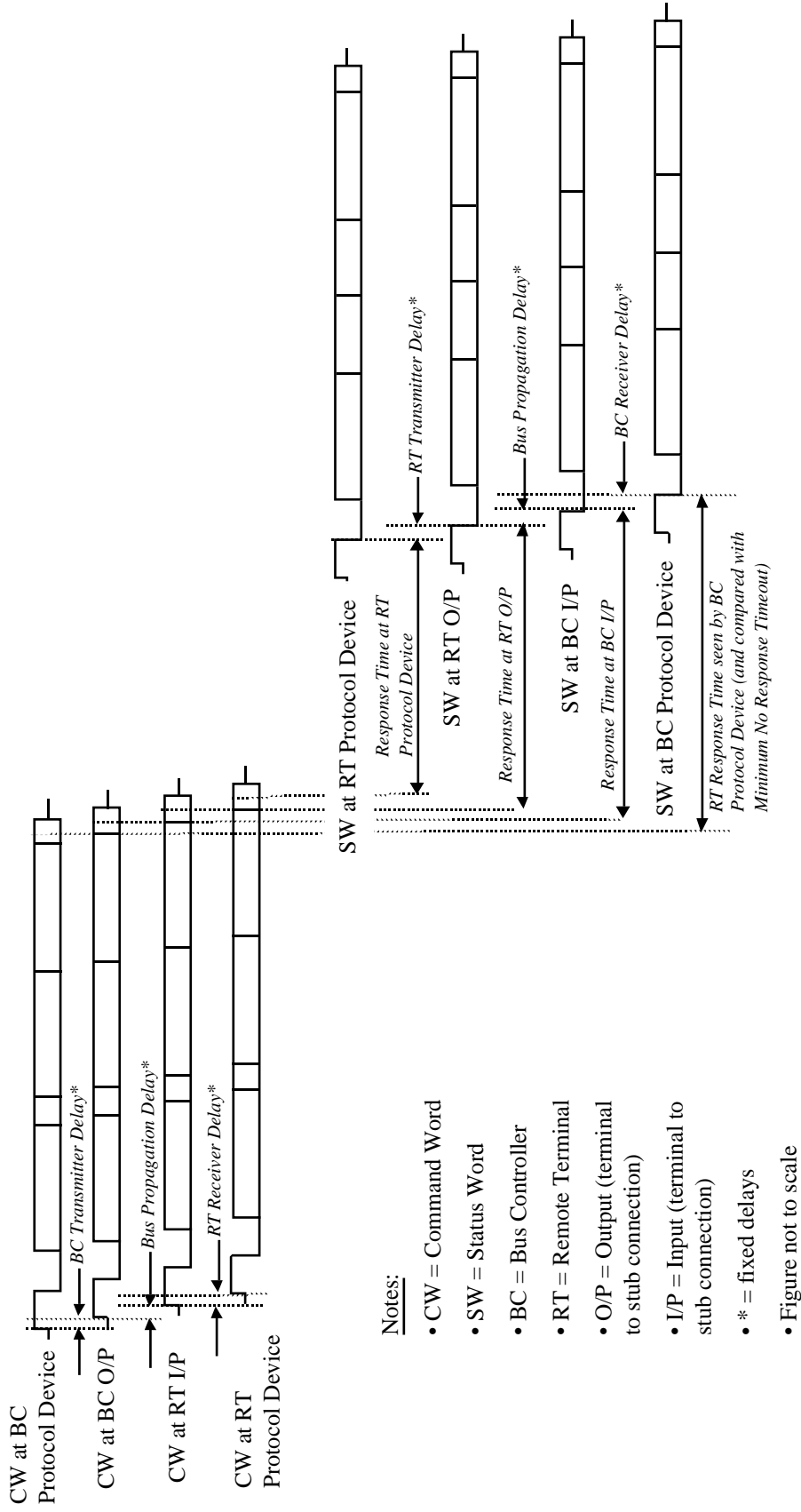


Figure 1: Effects of Transceiver and Bus Propagation Delays

Protocol Device Clock rate multiplier / Data rate (Mbits/s)	BC no resp timeout at Protocol Device t_{bcto_prot} (us)	BC Transceiver Delay (total for Tx & Rx) t_{trans} (us)	BC no resp timeout at stub $t_{bcto_stub} = t_{bcto_prot}$ - t_{trans} (us)	RT Response time at RT Protocol Device $t_{resp-prot}$ (us)	RT Transceiver Delay (total for Tx & Rx) t_{trans} (us)	RT Response time at Stub $t_{resp_stub} = t_{resp-prot} - t_{trans}$ (us)	Max Propagation Time = t_{bcto_stub} - t_{resp_stub} (us)	Max bus length (in m) for 5.28ns/m (1.6ns/ft)
1.000	14.750	0.750	14.000	11.250	0.750	12.000	2.000	189.394
2.000	7.375	0.750	6.625	5.625	0.750	6.375	0.250	23.674
3.000	4.917	0.750	4.167	3.750	0.750	4.500	-0.333	-31.566
4.000	3.688	0.750	2.938	2.813	0.750	3.563	-0.625	-59.186
5.000	2.950	0.750	2.200	2.250	0.750	3.000	-0.800	-75.758

Table 2: Timing Parameter Values for Various Data Rates – Extreme Case

Protocol Device Clock rate multiplier / Data rate (Mbits/s)	BC no resp timeout at Protocol Device t_{bcto_prot} (us)	BC Transceiver Delay (total for Tx & Rx) t_{trans} (us)	BC no resp timeout at stub $t_{bcto_stub} = t_{bcto_prot}$ - t_{trans} (us)	RT Response time at RT Protocol Device $t_{resp-prot}$ (us)	RT Transceiver Delay (total for Tx & Rx) t_{trans} (us)	RT Response time at Stub $t_{resp_stub} = t_{resp-prot} - t_{trans}$ (us)	Max Propagation Time = t_{bcto_stub} - t_{resp_stub} (us)	Max bus length (in m) for 5.28ns/m (1.6ns/ft)
1.000	16.750	0.750	16.000	9.250	0.750	10.000	6.000	568.182
2.000	8.375	0.750	7.625	4.625	0.750	5.375	2.250	213.068
3.000	5.583	0.750	4.833	3.083	0.750	3.833	1.000	94.697
4.000	4.188	0.750	3.438	2.313	0.750	3.063	0.375	35.511
5.000	3.350	0.750	2.600	1.850	0.750	2.600	0.000	0.000

Table 3: : Timing Parameter Values for Various Data Rates – More Probable Case

APPENDIX B - 'RADICAL' APPROACHES

This appendix briefly summarises the work being carried out (as of January 2000) by the SAE ASD AS1-A NG1553 Task Group on the operation of Def Stan 00-18 Part 2/US MIL-STD-1553B bus networks at enhanced data rates.

The charter of NG1553 is to identify and recommend a commercial standard that will run at 100Mbit/s, with the same level of determinism as Def Stan 00-18 Part 2/US MIL-STD-1553B, and operate on existing bus networks.

NG1553 has defined a network configuration known as the DeLong⁴ bus to be used as the basis for evaluation of proposed solutions.

As of May 2000 two potential solutions were under consideration by NG1553.

The first is based on study and exploitation of various modulation techniques developed by the telecommunications industry such as CAP, QAM, DMT and SDMT. All of these provide mechanisms for increasing the number of data bits transmitted per symbol, i.e. the code gain⁵. By utilising these techniques it is possible to achieve higher data rates without a corresponding increase in the spectral bandwidth of the transmitted signal. In this way much higher bit rates can be achieved within the bandwidth limitations imposed by the bus network. As of September 1999 a DMT DSL technique had been demonstrated achieving 11 Mbit/s over a 30m bus with a spectral bandwidth of less than 3 MHz. SDMT had achieved 51 Mbit/s over a 75m bus. However, it appears that these tests were performed on buses with just two stubs (one at each end). It is not clear whether a multidrop topology has been tested.

The second approach is based on an 'advanced transceiver' using proprietary digital filtering and equalisation techniques. As of September 1999 it was claimed that 100 Mbit/s had been achieved over a DeLong network model and that a similar bit rate would be demonstrated operating over a physical DeLong network in December 1999. It is claimed that 300 Mbit/s will be achievable using this technique with modified couplers. Documentation so far (May 2000) received from NG1553 only provides generalised information about the techniques used in the 'advanced transceiver'. It is not yet clear what modulation techniques, frequencies or signal amplitudes are used.

⁴ Named after a senior member of SAE ASD.

⁵ Manchester bi-phase encoding used in Def Stan 00-18 Part 2 / US MIL-STD-1553B provides just one bit per symbol.