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STUDY OF MAXIMUM SIGNALLING SPEED FOR ELECTRICAL DEF STAN 00-18 (PART 2)/US MIL-STD-1553B DATA BUSES

0 EXECUTIVE SUMMARY

The increased demands of modern avionic systems could benefit from an increase on the data throughput provided by DEF Stan 0018 (Part 2)/US MIL-STD-1553B bus networks. However, upgrading to new bus systems which involve the installation of new networks within the airframe would be extremely costly and time consuming, since de-skinning the airframe would often be required.

A very cost effective upgrade solution could he the operation of the electrical Def Stan 00-18 (Part 2)/US MIL-STD-1553B bus networks at higher signalling speeds without modification of the networks themselves.

This report describes a study aimed at determining the extent to which bit rate could be increased and consisting of four phases:

- an investigation of previous and current work on operation of 1553B bus networks at enhanced bit rates
- tests on typical bus hardware aimed at obtaining an indication of achievable bit rates
- a study of the effects on throughput of increasing word and message lengths beyond those defined in the standard
- a brief study of the theoretical capacity of a 1553B bus network and possible techniques for maximising its exploitation

The first phase identified work recently started at SAE in the USA on Next Generation 1553' part of which is concerned with utilisation of installed bus networks at enhanced bit rates. It also identified other relevant activities, by 1553B product suppliers, iii this area in the recent and more distant past.

The second phase consisted of carrying out tests on typical bus hardware with results that indicate that a significant and useful improvement in bit rate should be achievable.

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The study of the effects on throughput of increasing word and message lengths indicates that little benefit is likely to be achieved by till is approach.

The study of the theoretical capacity of a 1553B bus network gives an indication of the theoretical maximum bit rate, taking into account signal to noise ratio. It also suggests some techniques that might usefully be adopted to achieve enhanced bit rate, together with an estimate of the achievable bit rate.

Finally, suggestions are made for further steps towards the actual achievement of higher bit rate over installed 1553B bus networks.

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1. INTRODUCTION

This report sets out the results of a study into the potential for increasing the rate at which data is transmitted over existing DEF STAN 00-18 (Part 2)/MIL-STD 1553B data buses.

1.1 Background

The original signalling speed of the Def Stan 00-18 (Part 2) multiplex data bus was set at 1 Mbps with Manchester BI-phase coding employed to transmit clock and data information combined. This resulted in a complex waveform with virtually no dc component and primary frequency components of 500 kHz and 1 MHz in the transmitted waveform requiring a transfer medium bandwidth of at least 2 MHz.

The increased demands of modem avionic systems could benefit from an increased data throughput on the Def Stan 00-18 (Part 2)/US MIL-STD- 1553B bus networks. Upgrading to new bus systems which involved the installation of new networks within the airframe would be extremely costly and time consuming as dc-skinning the airframe would often be required.

A very cost effective upgrade solution could be the operation of the electrical Def Stan 00-18 (Part 2)/US MIL-STD-1553B bus networks at higher signalling speeds without modification of the networks themselves. This however might require development of terminal designs using modern silicon technology to obtain such improvements.

The most successful terminal designs capable of meeting the demanding noise rejection tests from the standard were based on receiver/decoder designs incorporating sampling front-ends operating in a range of 8 to 16 MHz. This was a demanding clock frequency using silicon technology employed when the 1553B hardware was first developed over a decade ago. However, modern silicon technology readily achieves much higher clock rates.

This report describes a study consisting of four phases:

- an investigation of previous and current work on operation of 1553B at enhanced bit rates
- tests on typical bus hardware aimed at achieving an indication of achievable bit rates
- a study of the effects on throughput of increasing word and message lengths beyond those defined in the standard
- a brief study of the theoretical capacity of a 1553B bus network and possible techniques for Maximising its exploitation.

2. ISSUES CONSTRAINING HIGH BIT RATE OPERATION

The physical constraints on high bit rate operation fall into three main areas as discussed below.

2.1 Terminal Electronics

2.1.1 Protocol and Encoder/Decoder Electronics

In order to achieve increased bit rate operation it is clearly necessary for protocol electronics to operate at higher speed. It is believed that for some existing products this would be simply a matter of increasing the clock frequency of the protocol logic. Other products may have constraints on maximum clock rate or other constraints that would prevent significant increases in operating speed.

2.1.2 Terminal Transceivers

Clearly transceivers would play a significant role in higher bit rate implementations. It is to be expected that transmitter rise and fall times and receiver filter characteristics would need consideration.

2.2 Bus Network Hardware

The fundamental objective of the study is to achieve an indication of the extent to which existing installed bus hardware could be used at higher bit rates than the standard 1 Mbps. All bus hardware elements might be expected to influence the outcome i.e. the bus cable, coupling transformers, isolation resistors and the interaction between these parts.

3. WORK ALREADY UNDERTAKEN OR CURRENTLY IN HAND

A number of organisations were contacted about previous work carried out on the use of 1553B hardware at higher bit rates than the 1 Mbps standard. The results of these enquiries are set out in the following sections.

3.1 SAE

A report on the SAE AS-1 meetings in October 1996 from Magder Consultants (ASSC/110/3/134) summarises relevant SAE activities.

SAE AS-1 has set up a Next Generation 1553 (NG 1553) Task Group at the request of the USAF (ASC) to provide guidance on enhancements and/or expansions to MIL-STD-1553B. NG1553 is understood to be writing a white paper to define system requirements and investigate possible solutions to these goals, as of February 1997 the status of this paper is unknown.

The eventual output of the NG1553 effort will be an SAE AIR document summarising the results of the effort and the recommendations of the Task Group.

It has been recognised that before beginning the effort, it will be necessary to establish the requirements for the NG1553 system. This task will establish the ground rules for the study and will be based on the results of a survey of present and future MIL-STD-1553B users.

The first approach to be studied will involve minimal enhancements to the existing 1553B standard, with the goal being to keep changes to legacy equipment to a minimum. Various methods will be investigated, ranging from simply increasing the clock speed of existing hardware to progressively more drastic techniques. Techniques to be considered include the effect of changing to re-designed data bus couplers and minor protocol changes. Methods of increasing the addressing capability and message length will also be investigated at this time

The SAE had been forwarded a WPAFB document 'Implementing Platform Electronics (Avionics) IPE (A) Version 2.1. Technical Development Approach'. This document is understood to contain a requirement for 'Consideration of copper wire performance limitations of legacy systems.' Hence it is of direct interest but unfortunately is classified 'US Eyes only'.

In addition to the concept of minimal enhancements to the existing standard, the NG1553 Task group will investigate the impact of new high speed data bus networks on legacy systems. The Task Group will recommend 1553 system level requirements which should be retained in order to preserve within these new networks the same degree of system level control that is presently provided by 1553B. This task will also include liaison with other committees that are working on new high speed network standards.

As new higher speed data bus equipment finds its way into service, either by retrofit or new system installation, there will be instances where a mix of new and legacy equipment must coexist within the same basic network. As the higher speed equipment becomes predominate, some legacy equipment will still be retained for a time before giving way to a new all-high-speed system. During this transition, methods must be provided to ensure compatibility between Next

Generation and Legacy equipment. The NG1553 task group will investigate methods for an orderly accomplishment of this transition.

System implementations under consideration by NG 1553 are understood to include:

- A New Generation Remote Terminal (RT) data bus connected to a Current Generation 1553B RT data bus, via a converting Gateway.
- A common bus which had both New Generation RTs and Current Generation I 553B RTs present, but utilising a "dual capable" Bus Controller.

It is understood that NG1553 has requested UK co-operation and that Magder Consultants has agreed to forward relevant data to ASSC as received.

Efforts have been made by ERA to communicate with SAE NG1553, but as of February 1997 a response is still awaited.

3.2 MCE

MCE reported that tests had been performed on 1553B terminals in 1987. These tests had been carried out using standard BC and RT chip sets with the clock frequency increased from l6 MHz to 32 MHz to achieve a 2 Mbps data rate. It was believed that the protocol devices would have operated at higher bit rates, but the terminal operation was limited by the behaviour of the receiver element of the transceivers believed to be due to the filters.

MCE were assured by the transceiver manufacturer that it would be relatively easy to change the receiver filter to permit operation tip to 4 Mbps.

The terminals used in the tests were constructed using multiple chip protocol devices fabricated using a 4 micron CMOS process. At the time of the test it was firmly believed that the single chip monolithic terminals then in development would have no problem working at 4 Mbps. Since then 1.2 micron products have been developed, which should be able to operate at still higher bit rates, although no tests have been carried out.

MCE said that experiments could be carried out on the present generation of devices, but resourcing such activities could be a problem.

3.3 CMAC

CMAC confirmed that 2 Mbps transceivers had been supplied to MCE in 1987 and 4 Mbps capability had also been demonstrated.

CMAC had also done some tests on bits networks using transceivers with modified receiver filters these had indicated a bus hardware imposed limit of about 4 to 5 Mbps.

Transmitter rise times could be reduced to about 100 ns for higher bit rate operation, but short rise times could lead to ringing at the ends of messages. CMAC also pointed out that transceivers have a propagation delay of about 500 ns which would remain roughly constant when receiver filters were modified. This could become a problem if response times were required to be scaled to increased bit rates.

CMAC said that it might be possible to carry out simple modifications to transceivers which could then be loaned for tests. However, significant modifications would be costly and require funding.

The possibility of using sine wave drivers was discussed and CMAC stated that sine wave transmitters use a filter to convert square waves to sine waves. If attempts were made to use sine wave transmitters designed for 1 Mbps at higher bit rates then the transmitter output amplitude would fall off at about 6 dB per octave as frequency I bit rate was increased.

CMAC stated that work had been carried out in collaboration with a US company on a SPICE model of a 1553B bus and it might be made available for investigations.

3.4 DDC

DDC in the US stated that a 10 Mbps system had been shipped 'many years ago'. This used coaxial cable and modified transformers together with GaAs transceivers.

Other tests had also been carried out 'a long time ago' using increased protocol chip clock rates and modified transceiver filters and a bit rate of 4 Mbps had been achieved.

No detailed information on the above was available after the lapse of time.

3.5 UTMC

UTMC was contacted because of a magazine article which mentioned work on a 20 Mbps terminal.

UTMC stated that the objective had been to implement a copper medium AS 1773 dual bit rate (1 Mbps and 20 Mbps) system with a 300' bus. 300' was chosen because this was the bus length specified in MIL-STD-1553A. The coupling transformers used were to a modified design to accommodate high bit rate operation.

Manchester hi-phase encoding was used, but had been found unsatisfactory due to low signal to noise ratio at the far end of the bus resulting in unacceptable bit error rates. It was felt that this problem could be overcome using a different modulation scheme such as frequency shift keying, or if a shorter bus was used. Consideration had been given to producing a 'smart transceiver capable of translating Manchester to (say) frequency shift keying modulation, but no funding was available for the work.

A dual 1 Mbps/20 Mbps A51773 protocol device (UT6916 ASCENT) had been produced by UTMC and customers were planning to use this in fibre implementations.

UTMC is involved in SAE AS-3 work on A51773, and reported that while the standard is media independent, effort is being concentrated on fibre implementations, with NASA, JPL and USN Research Labs pushing for satellite applications. Test plans have or are being prod used for fibre systems. There is no physical specification for wire AS 1773 as yet.

USAF was believed to be interested in legacy systems but seemed to be simply keeping a watch on developments.

3.6 Conclusions re previous and current work

Parts of the work apparently planned by the SAE AS-1 NG1553 Task Group are of direct relevance to the objectives of the task reported herein, and NG 1553 has expressed a desire for liaison with the UK. However, NG1553's planned aims appear to range from use of existing bus networks at higher bit rates to the consideration of 'transitional systems' requiring more radical actions, and the group's priorities are not clear. Furthermore, the extent to which SAE members will resource the planned work is not clear

MCE and CMAC have both carried out investigations of high bit rate operation (albeit many years ago) and appear to be interested in co-operating in further work in this area.

DDC appears to have little current interest in this area, although work was done in the distant past.

Although relevant work has been done recently by UTMC, interest appears to be focused on AS 1773 and hence 20 Mbps, the investigation into driving copper at 20 Mbps indicated that it would not be possible to achieve acceptable error rates at this speed.

It is recommended that liaison be established with SAE NG1553. Consideration should also be given to co-operation with MCE and CMAC in further investigations using transceivers, with minor modifications, and protocol devices running at higher than standard clock rates.

4. PRACTICAL TESTS ON BUS NETWORKS

4.1 Overview

The main objective of the programme of work is to determine the maximum bus signalling speed that can be achieved using a conventional electrical bus network meeting the requirements of the standard for bus cable, stub and coupling transformers.

Tests were performed on two bus assemblies one from Raychem, the other from Amphenol. The Raychem network consisted of a 10 m bus with 8 stubs. The Amphenol of a 40m bus with 9 stubs.

The tests consisted principally of injecting square and sine wave signals at a variety of frequencies into various stubs and recording the resultant signals at other points on the bus. The most important objective was to achieve an indication of the maximum frequency at which the minimum stub voltage as defined by the standard could be achieved at all points on the bus. Tests indicated that the frequency can be increased to about 6 MHz before this limit is reached. Tests also indicated that the effect of inserting a short circuit at various stubs was small. In some cases with the Amphenol bus when signals were injected at the centre of the bus a small increase in amplitude was observed when shorts were inserted.

The results suggest the that bus networks tested could be made to work with bit rates of up to about 6 Mbps. However, this does not give an indication of probable bit error rate, this is discussed further in Section 6 below.

Bus length is clearly an important constraint on maximum bit rate, but to date no indication has been identified as to the lengths buses typically in use. Such information would be valuable in estimating the extent to which bit rate could be increased.

Tests on the Raychem bus indicated that the effects of the strip cable through which the signals passed were minimal arid that the couplers also had little effect on signal amplitude. This agrees with the findings of UTM reported in Section 3.5 above.

Tests were also performed on the Am phenol bus which indicated that the bus provides a linear transfer function. This is an important issue in determining probable maximum bit rate and the feasibility of various techniques for achieving higher bit rate signalling as discussed in Section 6 of this report.

4.2 Practical Test Conclusions

The main conclusions to be drawn from the tests are that it is probable that buses could be successfully run at significantly greater bit rates than the standard 1 Mbps by simply increasing the bit rate while retaining the current encoding scheme.

It is desirable that further work be done to:

- determine bus lengths typically in use in aircraft
- further identify which bus hardware elements contribute to signal attenuation at high frequencies
- investigate the effects, if any, of the various lower frequency components in Manchester coding in determining the maximum bit

5. EFFECTS OF CHANGING WORD/MESSAGE LENGTHS

5.1 Overview

While the gross bit rate of a Def Stan 00-18 (Part 2) system is 1 Mbps the [1]useful information rate is significantly less because of the overhead imposed by command and status words, response times, intermessage gaps, data word synchronisation patterns and parity bits. The 'useful information' rate also varies with message length, increasing with the number of words in the message. Finally, the efficiency (i.e. ratio of time taken up in information transfer to total time per message) is different for various message formats being greatest for broadcast BC to RTs formats and lowest for RT to RT formats.

The 'useful information rate for a 32 data word BC to RT message at 1 Mbps may be calculated as 0.74 Mbps, assuming a response time of 12 microseconds and intermessage gap of 4 microseconds. The following sections discuss how the useful bit rate/efficiency could be enhanced by increasing data word length and/or message length while retaining 1 Mbps operation. Clearly these parameters could be modified in conjunction with increased bit rate, if this were done the results would be as given below but increased pro-rata with bit rate.

5.1.1 Word Lengths

Def Stan 00-18 (Part 2) defines words as consisting of a 3 microsecond synch period followed by 16 bits plus 1 parity bit. A greater throughput could be achieved if the number of information bits in each data word was increased.

Figure 1 shows a plot of Useful Bit Rate v Bits per Data Word for a stream of 32 data word messages.

It will be seen that relatively little benefit is achieved by this approach. For example increasing the word length from 16 to 32 data bits would increase the throughput from 0.74 to 0.85 Mbps i.e. by 14%. As word length is increased still further the curve patterns off indicated a reducing rate of improvement so that at a word length of 64 data bits the throughput is 0.92 Mbps an increase of 24% over the 16 bit case.

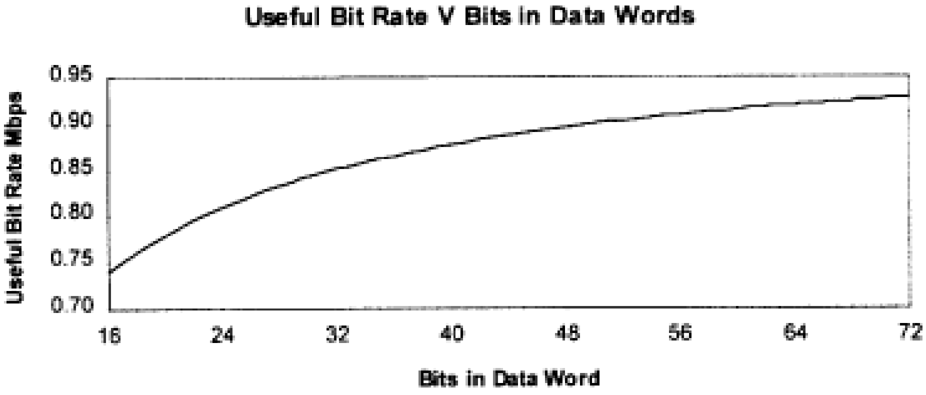

Fig. 1

5.1.2 Message Lengths

Def Stan 00-18 (Part 2) defines data transfer messages including up to 32 data words plus one command word one status word plus response time and intermessage gap time. A greater throughput could be achieved if the number data words in each message was increased.

Figure 2 shows a plot of Useful Bit Rate v Number of Data Words in a message for a stream of messages all with the given message length.

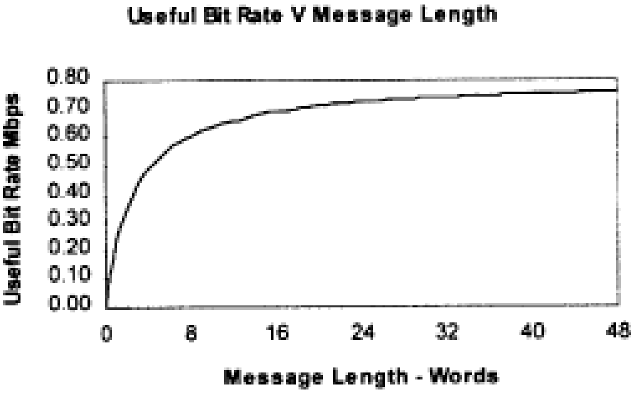

Fig. 2

It will be seen that the benefit achieved by this approach is even less than by increasing word length. Calculations show that increasing the message length from 32 to 64 data words increase the throughput from 0.74 to 0.77 Mbps i.e. by only 4%. Indeed the message length could be reduced to 16 words with only light reduction in throughput (7%) potentially freeing up a command word word-count bit for some other purpose.

5.1.3 Word/Message Length Combined

Figure 3 attempts to show the combined effect of data word length and message length on efficiency. It can be seen that increasing word length only has a significant effect on efficiency (or throughput) for short messages. For example in a one word message the efficiency is doubled from 0.28 to 0.57 if the word length is increased from 16 to 64 bits. Whereas for an eight word message the efficiency is increased by only 26% and as message length is increased still further the benefit from increased word length lessens still more soon becoming negligible. Conversely, if word length is kept constant and message length increased then there is initially a significant increase in throughput, but the rate of this improvement rapidly diminishes and is becoming negligible by the time the currently specified maximum message length of 32 data words is reached.

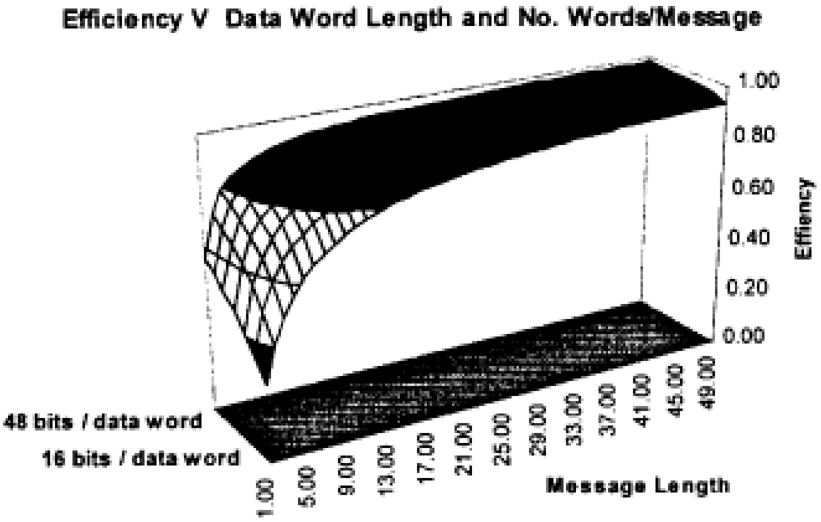

Fig. 3

5.1.4 Word/Message Length Conclusions

It appears from the above that there is little advantage to be gained in terms of throughput from modifying the word or message lengths. Furthermore, such modification would entail major changes to terminal hardware. Moreover, an increase in data word length would result in a reduction in the robustness of the system since, unless additional error detection was added, the data word parity bit would be protecting an increased number of bits.

6. 1553B CAPACITY LIMIT STUDY

The capacity limit C (bits/s), of a channel of bandwidth B (Hz), with Signal to Noise Ratio (S/N) is given by Shannon's law [2]:

$$C = B \log_2 (1 + S/N)$$

Tests made during the study confirm that the effective bandwidth of the 1553B bus is approximately 4 MHz. The noise tests included in the 1553B specification suggest that the worst case noise scenario is 140 mV pk-pk. The minimum signal level is 1 V pk-pk. This suggests that the theoretical maximum capacity of the 1553B data link is 22.8 Mbps/s.

The Shannon limit is notoriously difficult to achieve in any communication system. Nevertheless the limit is considerably higher than the current data rate of 1 Mbps/s which suggests there is considerable room for improvement. The following sections suggest some of the techniques that could be used to achieve higher data rates, closer to the Shannon limit.

6.1 “Turbo Charge” Existing System

The experiments with the test 1553B circuit show that significant attenuation occurs above 4 MHz. This suggests that the methods used already will continue to work when the data rate is turbo charged up to 2-4 MB/s. The received signal will be "smoothed", with no visible edges. Nevertheless, simple level detection at the bit period should work, with a slightly poorer error rate.

The drawback of running at faster data rates is the higher attenuation of signals and more noise power in the increased bandwidth of the receiver. Signal to noise ratio is degraded, which will worsen the bit error rate. Also increased data rates will degrade FMC performance. The attenuated power of higher signals is radiated into the atmosphere as EMI. In a safety critical radio environment, this is not desirable.

Running the system at even higher data rates than 4 MHz has been studied during the experimental stage of this project and by Slouch (Ref I). In [I] experiments are documented to show 20 Mbps data transfer over a 1553B bus. The shape of the digital data becomes unrecognisable, due to inter-symbol interference at these higher data rates. This is a classic adaptive filter problem and with the advances in DSP components in recent years is now solvable.

In order to find the characteristic inter symbol spreading of the channel, a known training sequence is passed over the channel. The analysis of the received training sequence shows the receiver how to adapt the matched filter to the conditions in the channel. As each 1553B installation is likely to be different, this means that the protocol must be changed to include the training sequence in all communications between bus entities. The training sequence needs to be a 16 or 32 bit pseudo random noise sequence.

Adding the training sequence to the protocol adds signalling overhead inefficiencies to the protocol. Also crudely driving the line faster than the design limit will increase EMI emissions.

Nevertheless this technique may offer the most cost effective means of higher rate data and should not be discounted.

6.2 Partial Impulse Response Modulation Schemes

In the previous section, we advocated letting the variable channel characteristics shape the signal to achieve high data rates. A potentially better solution is to deliberately shape the impulse response of the channel with a low pass data preconditioning filter. There are a number of advantages to this approach:

- No channel estimating training sequence is needed in the protocol.
- The FIR filter is still required to remove the inter-symbol distortion, but it no longer needs to be adaptive.
- The preconditioning filter will smooth the fast rise and fall times. This will ensure much better EMI performance.
- The approach provides a small amount of coding gain.

The last bullet merits explanation. When data is passed through a low pass filter, with a cut off frequency below the inverse of the bit period, (less than the data rate) the shape is distorted. Fig. 4 shows the effect. The lower the filter cut-oft, the smoother the output signal. It is important to note that the signal energy is not lost. It is spread in time. This action of spreading a data symbol actually provides some protection against errors. Noise spikes occur for a very short period, corrupting single bits of the energy of a data bit is spread across a number of bit periods instead of 1, it is more likely that the recovered data bit will be correct. This is the so called 'gain" that is obtained from spreading data bit over a number of bit periods.

The amount of gain available from this technique is not large and is dependent upon the error conditions in the channel and the filter cut off. A bandwidth (of the filter in Hz) bit period product (BT) of less than 1 is required to spread the data bit energy. BT = 0.2 would be required for a data rate of 10 MB/s or BT=0.1 for a data rate of 20 MB/s.

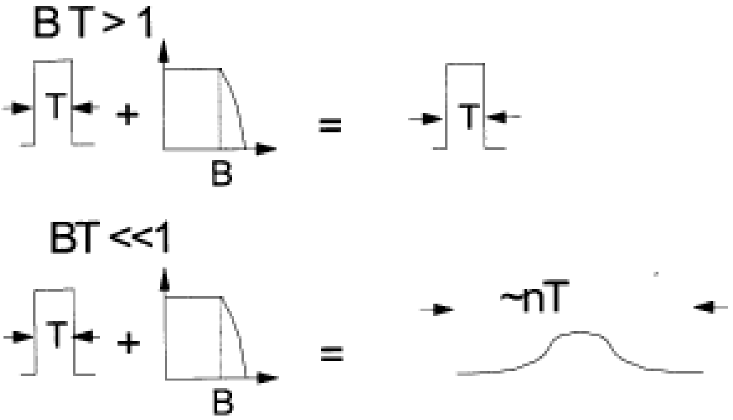

Fig. 4 Low pass filter effect

A BT product of 0.2 is achievable, but BT=0.1 may not be. It deserves further investigation.

6.3 Multi - level Schemes

A more sophisticated way of improving performance than increasing the data rate is to introduce a multilevel modulation scheme. In its crudest form this entails sending different amplitude signals to represent different states.

The existing modulation is binary, so it has a 1 bit symbol. If the transmitters and receivers are capable of receiving multiple levels, the symbol data content can be increased, without changing the required bandwidth or causing inter symbol interference. For example, if the levels are divided into 16, the effective data rate is quadrupled.

The major problem with this approach is that it requires a linear transmission system. Without a linear transmission system the relationship between different levels becomes distorted, causing errors in the receiver. Testing at ERA indicates that the system is linear in gain so these methods may be applicable. Nevertheless the gain and phase linearity must be characterised before implementing these types of solution.

A higher performance system can be implemented by using a signal "carrier". This is just a tone frequency onto which the data is modulated. This helps because the tone provides a reference for the receiver to measure the incoming signal against. This means that the receiver measures multiple levels against the carrier, rather than an absolute scale. Since the carrier has passed through the same channel as the signal, this relative assessment of levels will provide better performance.

Using a carrier also opens the possibility of implementing phase modulation schemes. Phase modulation is naturally more resilient to errors in the presence of noise. There are many type of phase modulation schemes, some which have amplitude modulation included also. The highest performance modems in telecommunication systems tend to implement Quadrature Amplitude Modulation (QAM).

In 16 QAM, the carrier signal phase and amplitude is quantised in 16 distinct detectable states, containing 4 bits of data, as shown in Fig. 5.

A carrier at 2 MHz with a modulation symbol rate of 1.5 Msps would fit the communication channel well. Thus 16 QAM would support 6 MB/s. Higher levels of QAM can be used to support higher data rates. In analogue telephone modems, 128 QAM is used to provide data rates up to 28.8 kBps through a 3 kHz channel.

The extra performance of the schemes brings some disadvantages. The complex nature of QAM modulation schemes complicate the receiver and transmitter hardware. More importantly, they have a lower SNR tolerance, and are more susceptible to distortion, leading to higher bit error rates.

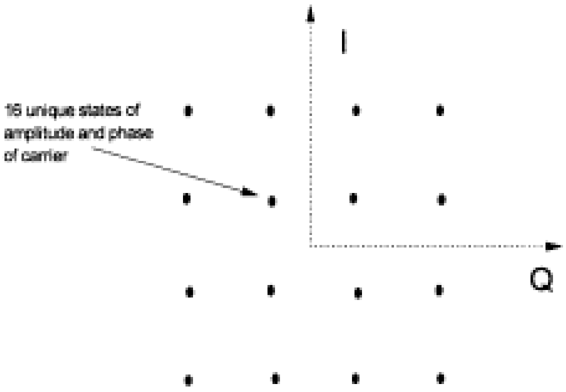

Fig. 5 The potential phase and amplitude states of a carrier modulated by 16 QAM, plotted in polar format

6.4 Managing Error Rates

The main concern raised in [l] is that the signal to noise ratio is degraded because of the attenuated signal. This is true and some of the techniques described above will also degrade the error rate, due to lower noise immunity of the modulation scheme. However it is important to note that in certain circumstances, the error rate can be managed by the use of an appropriate error coding scheme.

Coding schemes add redundancy to transmitted data that is used by the receiver to correct errors introduced by the transmission channel. Spectacular improvements in error rate can be achieved with modest error correction schemes. For example it is very easy to change a 10^{-3} error rate to 10^{-7} with a low rate code, tuned to the error conditions encountered in the channel.

Bus data transmissions are probably best suited to block type error coding. In this technique, a block of input data is passed through a code generator that translates the data to a longer coded block. For example, if a 100 bit data block is encoded using a 3/4 rate code, the coded block would be 133 bits. The additional 33 additional bits provide the measure of the error protection capability. In this case, up to 16 errors in the burst can be corrected, provided an optimal code is used.

Picking the code and the coding rate to use in any transmission scheme is very important. As can be seen from the above example, if more than 16 errors are likely to occur in a block, the whole block will be lost. If you get it wrong, it can make the error rate worse. Nevertheless, the ability to remove errors can be extremely powerful in reducing error rates.

Adding a coding scheme will add considerable complexity, especially at the data rates of interest (>>1 Mbps). Coding schemes can also add a delay, which is the length of the block for block codes. This may be undesirable in the 1553B application. There may be some scope to combine coding and modulation to provide better performance. The practicality of implementing decoders, or finding items off the shelf should be investigated further before pursuing this solution.

6.5 Performance Estimates

Assuming a Gaussian noise channel, to achieve an error rate of 10^{-7} using the existing Amplitude Shift Keying modulation requires a signal to noise ratio Eb/No >15 dB. This is consistent with the minimum signal level of 1 V pk-pk and worst case noise power of 0.14 V pk-pk, which gives Eb/No = 17 dB.

With an improved modulation scheme, the Eb/No can be reduced as low as 5 dB. If multilevel signals are used, the signal to noise, expressed in energy per bit is less. A 5 bit multilevel system will have dB SNR. The minimum acceptable. A 5 bit symbol, transmitted at 1.5 Msps suggests a maximum data rate of 7.5 Mbps.

Please note the 7.5 Mbps is critically dependent on the SNR ratio. If the signal power is attenuated due to higher frequency operation, this will critically affect the capacity.

6.6 Off the Shelf Solutions

High performance modems are used extensively in the telecommunications industry. Analogue PSTN modems are available that send 28.8 kbps data over many kilometres of twisted pair cable, in a bandwidth of 3 kHz. Higher data rates are also available, with some systems such as Asymmetric Digital Subscriber Line (ADSL) sending 2 Mbps over twisted pairs. These are mentioned as they indicate the availability of the modem technology to implement multi level modems. No attempt has been made to identify suitable components at this stage. Much more detail is required in the design of the system before it will be possible to tell whether specific components or chipsets are suitable for use in Fast 1553.

6.7 Summary

This section has tried to indicate what possibilities and limitations that exist for the speed of a Fast l553 data bus.

Turbo charging the existing data rate is simple. Better performance can be obtained from more advanced techniques, such as multi level and partial impulse response modulation schemes. The drawback is additional complexity and the need for the transmission media to be linear.

Shannon's law suggests a data rate >20 Mbps should be possible. Implementation problems always ensure that the effective data rate will be less than that. Signal to noise analysis suggests a maximum data rate of 7.5 Mbps is viable. This will not be simple to achieve and it might be wise to set a slightly more conservative target of 5 Mbps for a detailed feasibility study. More detailed study simulation and analysis is now required to provide more reliable answers.

References:

Scold (UTMC Micro Electronic Systems), (' an investigation into Using the MIL-STD-1553B Wire Bus at the AS-1773 20 Mbps Data Rate" .

Sklar, "Digital Communications Fundamentals and Applications", Prentice Hall International.

7. CONCLUSIONS

The study has achieved an indication of the extent to which bit rate could be increased on existing data bus networks, identified relevant current and previous work in this area, determined the effect of word and message lengths on throughput, investigated the limits on the capacity of 1553B bus networks and suggested advanced digital signal processing techniques that could be used to achieve enhanced bit rates.

The task has identified relevant previous and current work on the operation of data bus networks at high bit rate. The most important findings in this respect are:

- the work just starting at SAE, which promises useful liaison
- the work carried out recently at UTMC, which has provided an insight into attempts to operate buses at higher bit rate and over longer bus length than may be considered appropriate in terms of ASSC objectives
- the work done in the past by MCE and CMAC together with an apparent readiness to co-operate in future investigations.

The tests on bus networks have provided a first indication of bit rates that it might be achievable over installed buses.

Calculations on the effects of changing word and message lengths suggest that little benefit is to be achieved by this approach, particularly when the changes in terminal design that would be required are taken into account.

The study of the limits on the capacity of 1553B systems has provided some useful insight into the limitations on bit rate and also reviewed various techniques that might be adopted and the performance that might be achieved.

7.1 Future Steps

The work summarised above has shown that it is probable that a useful improvement in the bit rate transmitted over installed data bus networks could be achievable. It is recommended that further work be done to more closely quantify the this potential improvement and prove the capability. Ways in which this could be achieved include:

- further investigation into limitations on bandwidth with longer buses and more stubs
- implementation, in co-operation with terminal suppliers, of 'turbo charged' terminal electronics running at higher bit rates and with modified transceivers to carry out tests on bus hardware
- establishment of liaison with SAE NG1553 Task Group.